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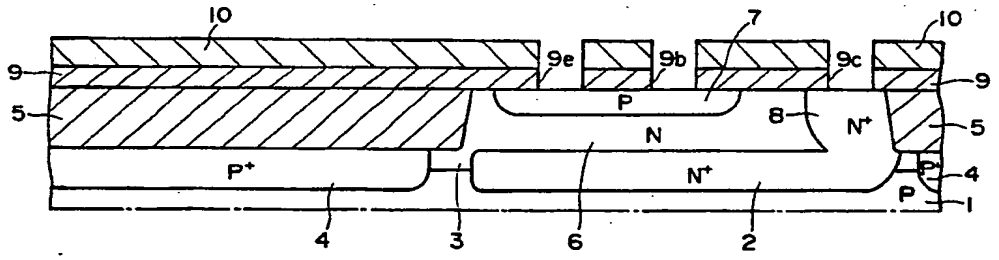
(54) Manufacture of semiconductor devices.

(57) A method of manufacturing a semiconductor device comprises forming a plurality of openings (9e, 9b, 9c) for ohmic contact portions at the same time, then forming a semiconductor layer (11) on an entire surface including the openings, and selectively introducing impurities by ion implantation into the contact portions and isolated other element regions (11e, 11b, 11c, 11t, 11R) of the semiconductor layer (11), thereby producing a transistor (Tr) and at least one other element (R; R, C).

FIG. 1B



EP 0 404 464 A2

MANUFACTURE OF SEMICONDUCTOR DEVICES

This invention relates to the manufacture of semiconductor devices.

In previously known bipolar transistor manufacturing methods, it has generally been customary to adopt procedures which comprise the steps of first forming a buried layer and an N-type epitaxial layer, and then double-diffusing impurities of first and second conduction types selectively into an active region which is surrounded by isolated inter-element regions, thereby forming a base region and an emitter region.

The latest developments of process technology have given rise to requirements for realising higher integration densities and higher operational speeds of the elements. For the purpose of meeting such requirements, it is usual to employ a polycrystalline silicon washed emitter (hereinafter referred to simply as a poly-washed emitter) structure. The use of a poly-washed emitter structure makes it possible to form a self-matched emitter region. Such structure contributes to a reduction in size of an emitter opening (which results in reduction of the cell size), and also to a decrease of base broadening resistance Rbb' which consequently results in advantages which allow obtaining a higher integration density and higher operational speeds of the elements.

A description of a previously proposed method for the manufacture of a bipolar transistor which has a poly-washed emitter structure will now be given with reference to Figures 3A to 3F of the accompanying drawings. First, as shown in Figure 3A, an N-type buried layer 32 and an N-type epitaxial layer 33 are formed on a P-type semiconductor substrate 31. Then, a P-type isolated inter-element region 34 and another isolated inter-element region 35 composed of a thick thermal oxide layer are formed. Then, a P-type impurity is selectively ion-implanted into an active region 36 which is surrounded by the isolated inter-element regions 34 and 35 to thereby form a base region 37. An N-type impurity is ion-implanted into a portion where a collector contact is to be formed, thereby forming a collector lead region 38 which extends to the buried layer 32. Subsequently, a silicon dioxide film 39 is formed by chemical vapour deposition (CVD) or the like on the entire surface inclusive of the active region 36.

Thereafter, as shown in Figure 3B, the silicon dioxide film 39 is selectively etched through a resist mask 40 so as to form open windows 39e and 39c in the portions corresponding to the emitter region (which will serve also as an emitter contact) and the collector contact of the active region 36.

In the next step, as shown in Figure 3C, the resist mask 40 on the silicon dioxide film 39 is removed, and a polycrystalline silicon layer 41 is formed on the silicon dioxide film 39 including the windows 39e and 39c. Thereafter, an N-type impurity (e.g. As^+) is ion-implanted into the polycrystalline silicon layer 41, and a heat treatment is performed so as to diffuse the N-type impurity from the polycrystalline silicon layer 41, thereby forming an emitter region 42e (which serves also as an emitter contact) and a collector contact 42c (which is represented by a broken line) in a self-matched state.

Subsequently, as shown in Figure 3D, the polycrystalline silicon layer 41 is patterned.

In the next step, as shown in Figure 3E, a resist mask 43 is formed on the polycrystalline silicon layer 41 and the silicon dioxide film 39, and then the silicon dioxide film 39 is etched through the resist mask 43 so as to form a window 39b at a position which corresponds to the base contact.

Subsequently, as shown in Figure 3F, an aluminium layer is formed on the entire surface after removal of the resist film 43, and the aluminium layer is patterned so as to form an emitter electrode 44e which is connected to the emitter region 42e through the polycrystalline silicon layer 41, a base electrode 44b which is connected to the base region 37, and a collector electrode 44c which is connected to the collector contact 42c through the polycrystalline silicon layer 41. A desired bipolar transistor is thus produced.

According to the above-described previously proposed method of manufacturing a bipolar transistor, the step of forming the windows 39e and 39c which are opposed to the emitter region 42e and the collector contact 42c is different from the step of forming the window 39b which is opposed to the base region 37, whereby a total of two resist masks (the above-mentioned masks 40 and 43) are required for opening the windows. Particularly when forming a composite device comprising a transistor, a resistor, a capacitor and so forth, a window opening resist mask is required for forming each element, which makes the window opening step complicated. Also, for ion-implantation, resist masks generally are required to be in conformity with the individual conduction types of the impurities, so that a multiplicity of resist masks are required for forming elements and these are additional to the aforementioned window opening resist masks, whereby the manufacture of a composite device becomes complicated.

It has recently been observed that, in accordance with a trend towards faster operation and

higher frequency band in the linear technical field for public use (including analog integrated circuits (ICs), analog large scale integration (LSI) devices, etc.), some devices have been proposed which utilise the poly-washed emitter type in the general linear process as well. For the purpose of improving the noise and frequency characteristics, it is desired that a metal-insulator-semiconductor (MIS) capacitor be employed as a filter. However, since a composite device is produced by a combination of different steps for the individual elements as described above, the steps become complicated and adverse influences occur due to heat treatment and so forth when forming other elements, which consequently causes a deterioration in the precision of control of the capacitance, thereby causing additional difficulties during manufacture (including the simultaneous production of an MIS capacitor for a transistor of a poly-washed emitter structure).

According to the invention there is provided a method of manufacturing a semiconductor device, the method comprising the steps of:
forming simultaneously s plurality of openings for ohmic contact portions in a surface layer of a semiconductor substrate;
forming a semiconductor layer over the entire surface layer including said openings for ohmic contact portions; and
selectively introducing impurities by ion implantation into contact portions and isolated other element regions of the semiconductor layer to produce a transistor and at least one other element.

Preferred embodiments of the invention described hereinbelow solve or at least alleviate the problems described above; and provide semiconductor device manufacturing methods which are capable of enabling simultaneous production of a transistor and at least one other element (such as a transistor of another type, and/or a resistor and/or a capacitor) in which the process steps during manufacture are simplified.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

Figures 1A to 1J illustrate sequential steps of a first method embodying the invention for manufacturing a composite semiconductor device;

Figures 2A to 2M illustrate sequential steps of a second method embodying the invention for manufacturing a composite device; and

Figures 3A to 3F illustrate sequential steps of a previously proposed method of manufacturing a bipolar transistor.

Figures 1A to 1J illustrate a first semiconductor device manufacturing method embodying the invention and, in particular, sequential steps in the method, which is for simultaneously producing an NPN type bipolar transistor of a poly-washed emitter structure and a resistor composed of polycrystalline silicon. The individual steps will be described sequentially.

First, as shown in Figure 1A, an N-type buried layer 2 and an N-type epitaxial layer 3 are formed on a P-type semiconductor substrate (e.g. a silicon substrate) 1, and then a P-type isolated inter-element region 4 and another isolated inter-element region 5 in the form of a thick thermal oxide layer (e.g. a silicon dioxide layer) are formed. Then, a P-type impurity is selectively ion-implanted into an active region 6 which is surrounded by the isolated inter-element regions 4 and 5, to thereby form a base region 7. Simultaneously, an N-type impurity is ion-implanted into a portion where a collector contact is to be formed, thereby forming an N-type collector lead region 8 which extends to the buried layer 2. Then, a silicon dioxide layer 9 is formed by chemical vapour deposition (CVD) or the like on the entire surface inclusive of the active region 6.

Subsequently, as shown in Figure 1B, a resist mask 10 is formed on the silicon dioxide film 9, and the film 9 is then selectively etched through the resist mask 10 to open, simultaneously (that is, in the same process (etching) step), windows 9e, 9b, 9c which correspond, respectively, to an emitter region (which serves also as an emitter contact), a base contact and the collector contact in the active region.

In the next step, as shown in Figure 1C, the resist mask 10 on the silicon dioxide film 9 is removed and a polycrystalline silicon layer 11 is formed by CVD or the like on the silicon dioxide film 9 including the windows 9e, 9b, 9c.

Subsequently, as shown in Figure 1D, a resist mask 12 is formed on the polycrystalline silicon layer 11, and a P-type impurity, such as a boronic impurity (e.g. B^+, BF_2^+), is ion-implanted through a window 12R of the resist mask 12 into a portion 11R which serves as a resistor part 11r constituted by the polycrystalline silicon layer 11.

Then, as shown in Figure 1E, the resist mask 12 on the polycrystalline silicon layer 11 is removed and another resist mask 13 is formed on the layer 11. Thereafter, a P-type impurity (e.g. B^+, BF_2^+) is ion-implanted through windows 13t, 13b of the resist mask 13 into resistor contact portions 11t of the polycrystalline silicon layer 11 and a portion 11b which corresponds to the base contact and later partially constitutes a base electrode.

Next, as shown in Figure 1F, the resist mask 13 on the polycrystalline silicon layer 11 is removed and a resist mask 14 is formed on the layer 11. Thereafter, an N-type impurity (e.g. As^+) is ion-implanted through windows 14e, 14c of the resist mask 14 into a portion 11e which corresponds to the emitter region of the polycrystalline silicon layer 11 and later partially constitutes an emitter elec-

trode, and a portion 11c which corresponds to the collector contact of the layer 11 and later partially constitutes a collector electrode.

Subsequently, as shown in Figure 1G, the resist mask 14 on the polycrystalline silicon layer 11 is removed and then a silicon dioxide film 15 is formed on the layer 11 by CVD or the like. The silicon dioxide film 15 functions as a cap film for preventing scattering of the impurities from the polycrystalline silicon layer 11 during heat treatment, which is to be performed during the next step, and also for preventing the mutual mixing of impurities of different conduction types. Thereafter, the heat treatment is performed. In this stage, the N-type impurities from both the portion 11e of the polycrystalline silicon layer 11 which corresponds to the emitter region and the portion 11c of the layer 11 which corresponds to the collector contact are diffused into the base region 7 and the collector lead region 8, which are located under such portions respectively, thereby forming an emitter region l6e and a collector contact 16c (shown by a broken line). Simultaneously, the P-type impurity from the portion 11b which corresponds to the base contact of the polycrystalline silicon layer 11 is diffused into the base region 7 so as to form a base contact 16b (shown by a broken line).

In the next step, as shown in Figure 1H, the cap silicon dioxide film 15 on the polycrystalline silicon layer 11 is entirely removed, and then the layer 11 is patterned. In this stage, the patterning is performed so as to leave the resistor part 11r, the resistor contact portions 11t, the portion 11e which corresponds to the emitter region 16e, the portion 11b which corresponds to the base contact 16b, and the portion 11c which corresponds to the collector contact 16c.

Subsequently, as shown in Figure 1I, a relatively thin Si_3N_4 film 17 is formed on the entire surface by decompressed CVD or the like, and then a relatively thick silicon dioxide film 18 is formed on the entire surface. Thereafter, the silicon dioxide film 18 is patterned so as to be partially left on the resistor part 11r and the resistor contact portions 11t. In this state, the Si_3N_4 film 17 functions as an etching stopper to prevent removal of the silicon dioxide film 9 which is located underneath it.

In the next step, as shown in Figure 1J, the Si_3N_4 film 17 is removed by etching with hot phosphoric acid or the like in a manner such that the portions which are under the silicon dioxide layer 18 are left. Thereafter, an aluminium layer is formed on the entire surface and is then patterned so as to form a pair of resistor electrodes 19t, an emitter electrode 19e, a base electrode 19b and a collector electrode 19c, thereby producing a composite device which comprises a bipolar transistor Tr of a poly-washed emitter structure and a resistor R.

A second method embodying the invention for simultaneously producing the above-described composite device and, also, an MIS capacitor will now be described with reference to Figures 2A to 2M, which illustrate sequential steps of the method. In Figures 2A to 2M, items which are the same as items in the first embodiment shown in Figure 1A to 1J are denoted by the same references.

First, as shown in Figure 2A, an N-type buried layer 2, an N-type epitaxial layer 3, isolated inter-element regions 4 and 5, a P-type region 7 and an N-type collector lead region 8 are formed on a P-type silicon substrate 1. Thereafter, a silicon dioxide film 9 is formed by CVD or the like on the entire surface inclusive of active regions 6a and 6b.

In the next step, as shown in Figure 2B, a resist mask 10 is formed on the silicon dioxide film 9, and the film 9 is then selectively etched through the resist mask 10 to open, simultaneously, (that is, in the same process (etching) step), windows 9e, 9b, 9c, 9g which correspond, respectively, to an emitter region (which also serves as an emitter contact), a base contact and a collector contact in the active region 6a, and one electrode lead region of the MIS capacitor in the active region 6b.

Thereafter, as shown in Figure 2C, the resist mask 10 on the silicon dioxide film 9 is removed and a polycrystalline silicon layer 11 is formed by CVD or the like on the silicon dioxide film 9 including the windows 9e, 9b, 9c, 9g.

In the next step, as shown in Figure 2D, a resist mask 12 is formed on the polycrystalline silicon layer 11, and a P-type impurity, such as a boronic impurity (e.g. B^+, BF_2^+), is ion-implanted through a window 12R of the resist mask 12 into a portion 11R which serves as a resistor part 11r constituted by the polycrystalline silicon layer 11.

Then, as shown in Figure 2E, the resist mask 12 on the polycrystalline silicon layer 11 is removed and another resist mask 13 is formed on the layer 11. Thereafter, a P-type impurity (e.g. B^+, BF_2^+) is ion-implanted through windows 13t, 13b of the resist mask 13 into resistor contact portions 11t of the polycrystalline silicon layer 11 and a portion 11b which corresponds to the base contact.

Next, as shown in Figure 2F, the resist mask 13 on the polycrystalline silicon layer 11 is removed and a resist mask 14 is formed on the layer 11. Thereafter, an N-type impurity (e.g. As^+) is ion-implanted through windows 14e, 14c, 14g of the resist mask 14 into a portion 11e of the polycrystalline silicon layer 11 which corresponds to the emitter region, a portion 11c of the layer 11 which corresponds to a collector contact, and a portion 11g of the layer 11 which corresponds to the one electrode lead region of the MIS capacitor.

Subsequently, as shown in Figure 2G, the resist mask 14 on the polycrystalline silicon layer 11 is removed and then the polycrystalline silicon layer 11 is patterned. In this stage, the patterning is performed so as to leave the resistor part 11r, the resistor contact portions 11t, the portion 11e which corresponds to the emitter region, the portion 11b which corresponds to the base contact, the portion 11c which corresponds to the collector contact, and the portion 11g which corresponds to the one electrode lead region of the MIS capacitor.

Next, as shown in Figure 2H, a relatively thin Si_3N_4 film 17 is formed on the entire surface by decompressed CVD or the like, and then a relatively thick silicon dioxide film 15 is formed on the Si_3N_4 film 17 by CVD or the like. In similar member to the first embodiment, the silicon dioxide film 15 functions as a cap film. Thereafter, heat treatment is performed. In this stage, the N-type impurities from the portion 11e of the polycrystalline silicon layer 11 which corresponds to the emitter region, the portion 11c of the layer 11 which corresponds to the collector contact, and the portion 11g of the layer 11 which corresponds to the one electrode lead region of the MIS capacitor are diffused into the base region 7, the collector lead region 8 and the active region 6b, which are located under such portions, respectively, thereby forming an emitter region 16e (which also serves as an emitter contact), a collector contact 16c (shown by a broken line) and the one electrode lead region 16g of the MIS capacitor. Simultaneously, the P-type impurity from the portion 11b of the polycrystalline silicon layer 11 which corresponds to the base contact is diffused into the base region 7 so as to form a base contact 16b (shown by a broken line).

Next, as shown in Figure 2I, the silicon dioxide film 15 is patterned so that the portions thereof on the resistor part 11r and the resistor contact portions 11t are left unremoved. In this stage, the Si_3N_4 film 17 functions as an etching stopper to prevent removal of the silicon dioxide film 9 which is located underneath it.

Subsequently, as shown in Figure 2J, the Si_3N_4 film 17 is etched with hot phosphoric acid or the like in a manner such that the portions located under the silicon dioxide film 15 are left.

In the next step, as shown in Figure 2K, a resist mask 20 is formed on the entire surface, and the silicon dioxide film 9 is then selectively etched through the resist mask 20 to open a window 9m which communicates with the active region 6b and determines the capacitance (area) or the MIS capacitor.

Next, as shown in Figure 2L, a Si_3N_4 film 21 which is thicker than the Si_3N_4 film 17 is formed on the entire surface by decompressed CVD or the like, and the film 21 is then patterned so that the portion of the film 21 which corresponds to the window 9m is left. The Si_3N_4 film 21 is used as a dielectric film of the MIS capacitor.

Thereafter, as shown in Figure 2M, an aluminium layer is formed on the entire surface and is then patterned so as to form a pair of resistor electrodes 19t of the resistor part 11r, an emitter electrode 19e, a base electrode 19b, a collector electrode 19c, an electrode 19g of the MIS capacitor, and another electrode 19m of the MIS capacitor, thereby producing a composite device which comprises a bipolar transistor Tr of a poly-washed emitter structure, a resistor R and an MIS capacitor C.

According to this embodiment, as described above, windows 9e, 9b, 9c which correspond to ohmic contacts of a transistor, i.e. an emitter region 16e, a base contact 16b and a collector contact 16c, and also another window 9g which corresponds to an ohmic contact of the MIS capacitor, i.e. one electrode lead region 16g of the MIS capacitor (as shown in Figures 1B and 2B), can be formed at the same time. After a polycrystalline silicon layer 11 is formed on the entire surface including the windows 9e, 9b, 9c, 9g which correspond to such ohmic contacts, P-type and N-type impurities are selectively introduced by ion implantation into the portions 11e, 11b, 11c, 11g of the layer 11 which correspond to the ohmic contacts and the isolated other element region 11R, whereby the resistor R and the MIS capacitor C can be produced simultaneously with the bipolar transistor Tr. Furthermore, since only a single resist mask (the mask 10) is required for forming the windows 9e, 9b, 9c, 9g which correspond to the ohmic contacts, the steps of forming the ohmic contacts are simplified. Particularly in the case of simultaneously producing the MIS capacitor C therewith, the step relating to the capacitor C can be executed in the final stage as shown in Figure 2L, so that any adverse (harmful) influences resulting from heat treatment and so forth (shown in Figure 2H) are prevented (that is, the dielectric constant of the Si_3N_4 film 21 which serves as the dielectric film is not affected), thus producing a satisfactory MIS capacitor with high precision of control of the capacitance.

In addition, as described in connection with the second embodiment where the polycrystalline silicon layer 11 is patterned immediately after the step of ion implantation (shown in Figures 2D to 2F), the cap silicon dioxide film 15 formed thereafter can be patterned without being entirely removed and can therefore be utilised as an interlayer insulator film for the resistor contact portions 11t. Consequently, it becomes possible to eliminate the double operation of first forming the cap silicon

dioxide film 15 as in the first embodiment and, after the heat treatment, removing the entire cap silicon dioxide film 15, then forming a silicon dioxide film 18 again and patterning it to obtain an interlayer insulator film for the resistor contact portions 11t.

Also, with regard to the step of ion implantation, an advantage is obtained in that, since the ion implantation is executed into the substrate where the element regions and the windows corresponding to the entire ohmic contacts relative to the elements have previously been formed, the ion implantation for the individual conduction types as a whole ranges from a minimum of twice (once for P-type and once for Ntype) to a maximum of four times (twice for P-type and twice for Ntype), so that the steps of ion implantation can be simplified. In this embodiment, the ion implantation is repeated only a total of three times (twice for P-type and once for N-type).

Also, the polycrystalline silicon layer 11 can be used to obtain both a polycrystalline silicon layer which is used for forming the resistor part 11r, the resistor contact portions 11t and the portion 11g corresponding to one electrode lead region 16g of the MIS capacitor, and another polycrystalline silicon layer which is used for forming the contacts to the diffused regions 16e, 16b, 16c of the bipolar transistor Tr. Therefore, all of the contact portions can be formed out of the single polycrystalline silicon layer 11 during one patterning step, hence simplifying the process for shaping the contact portions.

The first embodiment relates to the simultaneous production of an NPN-type bipolar transistor Tr and a resistor R; while the second embodiment relates to the simultaneous production of an NPN-type bipolar transistor Tr, a resistor R and an MIS capacitor C. However, a PNP-type bipolar transistor may be produced in place of the above NPN-type bipolar transistor, or a MOS transistor may be produced as well. Furthermore, it is possible to simultaneously produce a bi-MOS transistor or a bi-CMOS transistor with a resistor and a MIS capacitor.

According to the above-described semiconductor device manufacturing methods embodying the invention, windows corresponding to ohmic contacts are opened at the same time and, after a semiconductor layer is formed on the entire surface including such open windows, impurities are selectively introduced by ion implantation into the portions of the semiconductor layer which correspond to the contacts and the isolated other element region to produce a transistor and at least one other element. Consequently, simultaneous production of a transistor and other elements (e.g. resistor and capacitor) can be realised with a simplified process of manufacture.

Claims

1. A method of manufacturing a semiconductor device, the method comprising the steps of:
forming simultaneously s plurality of openings (9e, 9b, 9c; 9e, 9b, 9c, 9g) for ohmic contact portions in a surface layer (9) of a semiconductor substrate (1);
forming a semiconductor layer (11) over the entire surface layer including said openings for ohmic contact portions; and
selectively introducing impurities by ion implantation into contact portions and isolated other element regions (11e, 11b, 11c, 11t, 11R; 11e, 11b, 11c, 11g, 11t, 11R) of the semiconductor layer (11) to produce a transistor (Tr) and at least one other element (R; R, C).

2. A method of manufacturing a transistor (Tr) and at least one other device (R), the method comprising the steps of:
forming N and P regions (2, 3, 4, 6, 7, 8), including a base region (7) and a collector lead region (8), in a substrate (1);
forming an insulating film (9) on a surface of the substrate (1);
forming a first resist mask (10) on the insulating film (9);
selectively etching the insulating film (9) through the first resist mask (10) to form a plurality of windows (9e, 9b, 9c) to the substrate (1);
removing the first resist mask (10);
forming a polycrystalline layer (11) on the insulating film (9) and in the plurality of windows (9e, 9b, 9c);
forming a second resist mask (12) on the polycrystalline layer (11);
ion-implanting a P-type impurity through a window (12R) of the second resist mask (12) into a portion (11R) which will be a resistor part (11r) of the polycrystalline layer (11);
removing the second resist mask (12);
forming a third resist mask (13) on the polycrystalline layer (11);
effecting ion-implantation through windows (13t, 13b) of the third resist mask (13) to form resistor contact portions (11t) and a base contact portion (11b) which will correspond to a base in the polycrystalline later (11);
removing the third resist mask (13);
forming a fourth resist mask (14) on the polycrystalline layer (11);
effecting ion-implantation through windows (14e, 14c) of the fourth resist mask (14) into portions (11e, 11c) of the polycrystalline layer (11) which correspond to an emitter region and a collector

contact:
removing the fourth resist mask (14);
forming another insulating film (15) on the polycrystalline layer (11);
heat treating the substrate structure and diffusing on N-type impurity from the portions (11e, 11c) of the polycrystalline later (11) which correspond to the emitter region and the collector contact into the base region (7) and the collector lead region (8), respectively, to form the emitter region (16e) and the collector contact (16c) and simultaneously diffusing a P-type impurity from the base contact portion (11b) of the polycrystalline layer (11) into the base region (7) to form a base contact (16b);
removing the other insulating film (15);
forming patterns in the polycrystalline layer (11) to leave the resistor part (11r), the resistor contact portions (11t), the portion (11e) which corresponds to the emitter region (16e), the base contact portion (11b) and the portion (11c) which corresponds to the collector contact (16c);
forming a thin film (17) on the patterned polycrystalline layer (11);
forming a relatively thick insulating film (18) on the thin film (17);
patterning the relatively thick insulating film (18) so that it is partially left on the resistor part (11r) and the resistor contact portions (11t); and
forming resistor electrodes (19t), an emitter electrode (19e), a base electrode (19b) and a collector electrode (19c).

3. A method of manufacturing a transistor (Tr) and at least two other devices (R, C), the method comprising the steps of:
forming N and P regions (2, 3, 4, 6a, 6b, 7, 8), including a base region (7), a collector lead region (8) and an active region (6b), in a substrate (1);
forming a first insulating film (9) on a surface of the substrate (1);
forming a first resist mask (10) on the insulating film (9);
selectively etching the insulating film (9) through the first resist mask (10) to form a plurality of windows (9e, 9b, 9c, 9g) to the substrate (1);
removing the first resist mask (10);
forming a polycrystalline layer (11) on the insulating film (9) and in the plurality of windows (9e, 9b, 9c, 9b);
forming a second resist mask (12) on the polycrystalline layer (11);
ion-implanting a P-type impurity through a window (12R) of the second resist mask (12) into a portion (11R) which will be a resistor part (11r) of the polycrystalline layer (11);
removing the second resist mask (12);
forming a third resist mask (13) on the polycrystalline layer (11);
effecting ion-implantation through windows (13t, 13b) of the third resist mask (13) to form resistor contact portions (11t) and a base contact portion (11b) which will correspond to a base in the polycrystalline layer (11);
removing the third resist mask (13) ;
forming a fourth resist mask (14) on the polycrystalline layer (11);
effecting ion-implantation through windows (14e, 14c, 14g) of the fourth resist mask (14) into portions (11e, 11c, 11g) of the polycrystalline layer (11) which correspond, respectively, to an emitter region, a collector contact and a lead of a capacitor (C);
removing the fourth resist mask (14);
patterning the polycrystalline layer (11) to leave the resistor part (11r), the resistor contact portions (11t), the portion (11e) corresponding to the emitter region, the base contact portion (11b), the portion (11c) corresponding to the collector contact and the portion (11g) corresponding to the lead of the capacitor ;
forming a thin film (17) on the substrate structure;
forming a second insulating film (15) on the thin film (17);
heat treating the substrate structure and diffusing an N-type impurity from the portions (11e, 11c, 11g) of the polycrystalline layer (11) which correspond to the emitter region, the collector contact and the capacitor lead into the base region (7), the collector lead region (8) and the active region (6b), respectively, to form the emitter region (16e), collector contact (16c) and one lead of the capacitor (C), and simultaneously diffusing a P-type impurity from the base contact portion (11b) of the polycrystalline layer (11) into the base region (7) to form a base contact (16b);
patterning the second insulating film (15) to leave the resistor part (11r) and the resistor contact portions (11t);
patterning the thin film (17) so that the portions under the second insulating film (15) remain;
forming a fifth resist mask (20) on the substrate structure;
selectively etching the first insulating film (9) to open a further window (9m) which communicates with the active region (6b) and determines the capacitance of the capacitor (C);
forming a further film (21) on the substrate structure;
patterning the further film (21) so that a portion of the film (21) which corresponds to the further window (9m) is left; and
forming electrodes (19t) for the resistor part (11r), an emitter electrode (19e), a base electrode (19g), a collector electrode (19c) and two capacitor electrodes (19g, 19m).

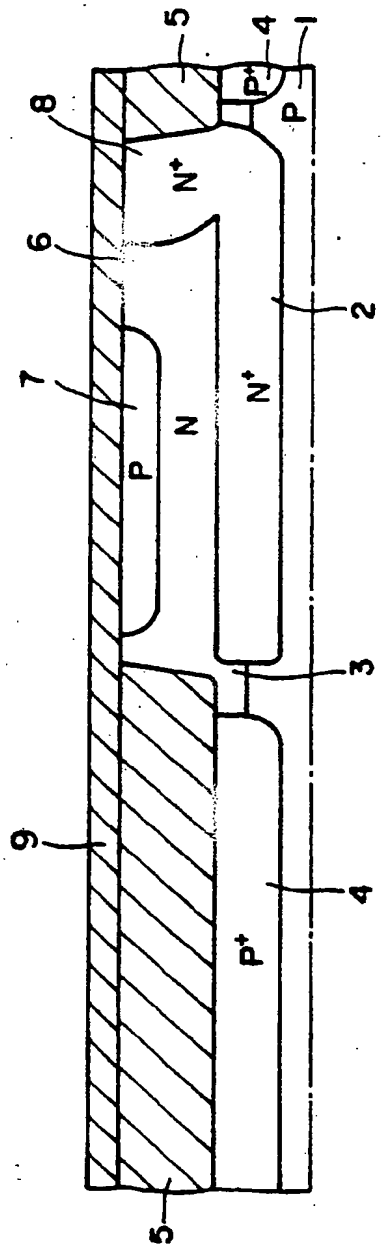


FIG. 1A

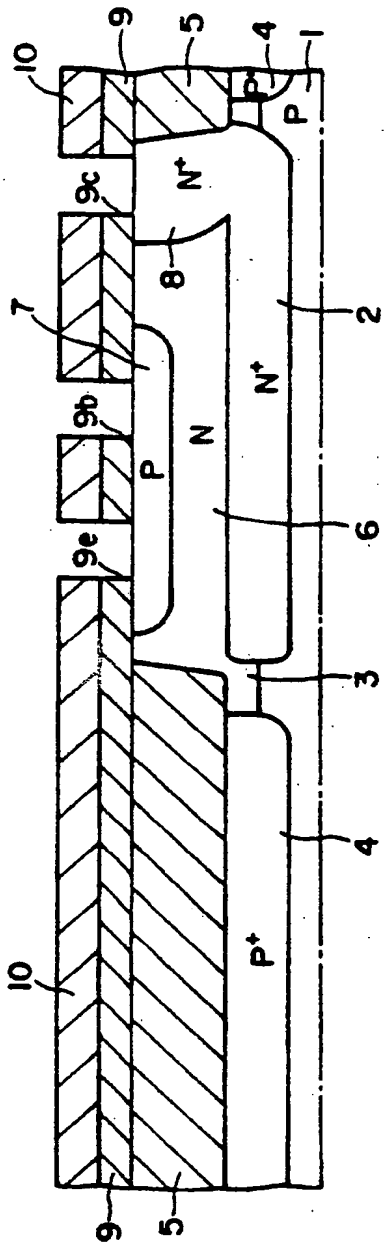


FIG. 1B

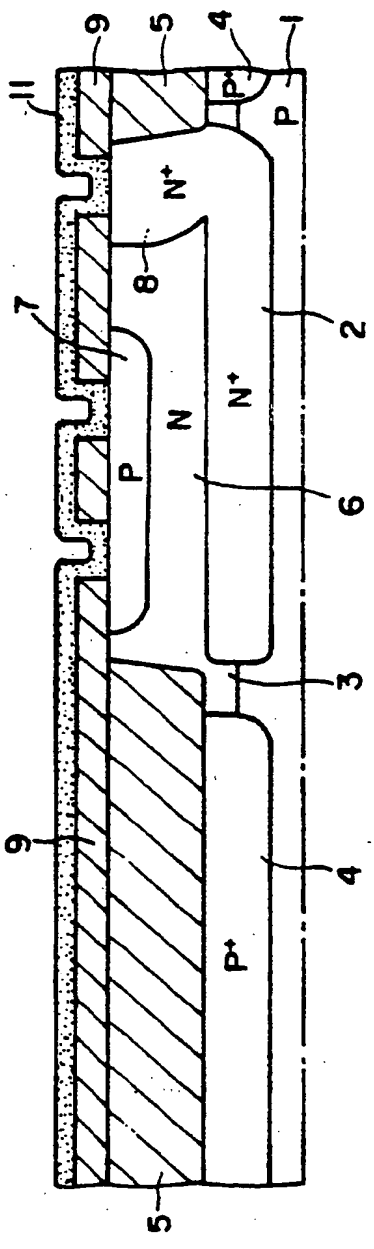


FIG. 1C

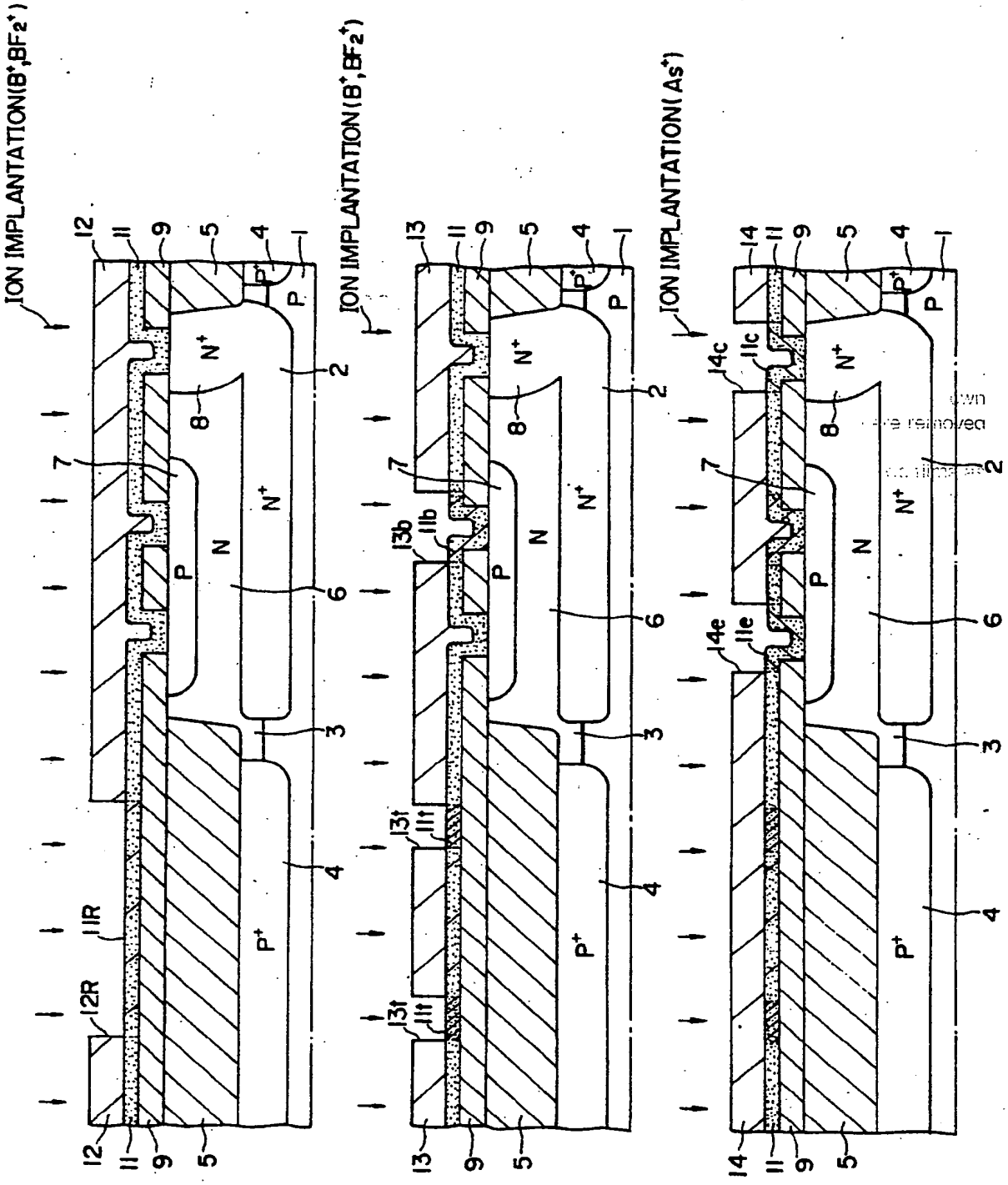


FIG. 1D

FIG. 1E

FIG. 1F

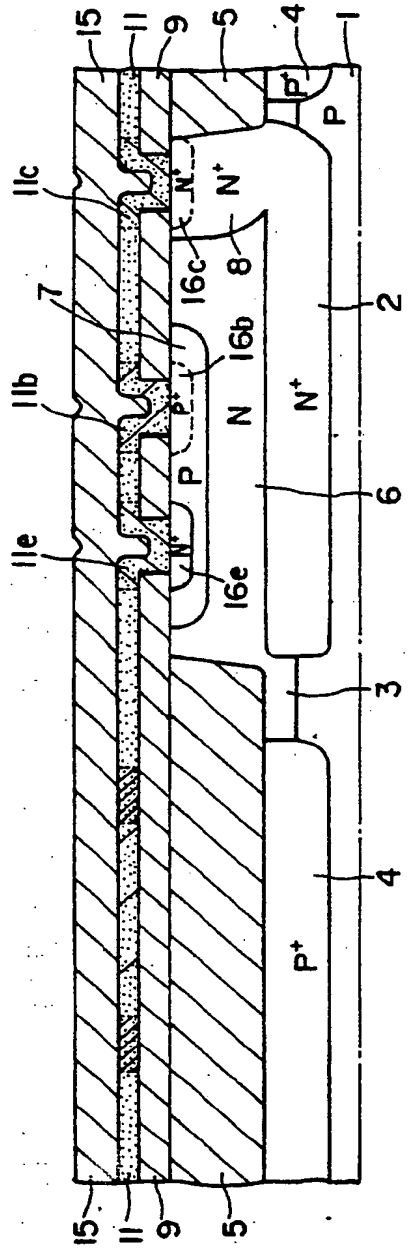


FIG. 1G

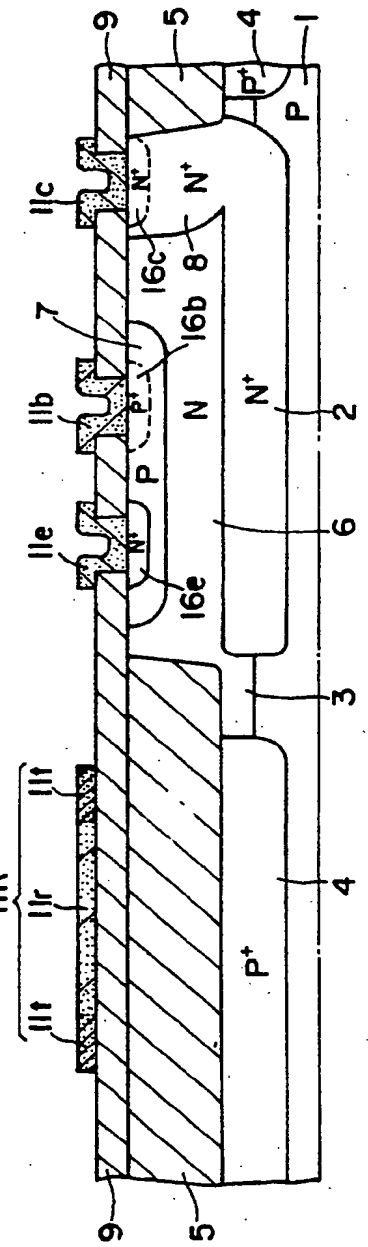


FIG. 1H

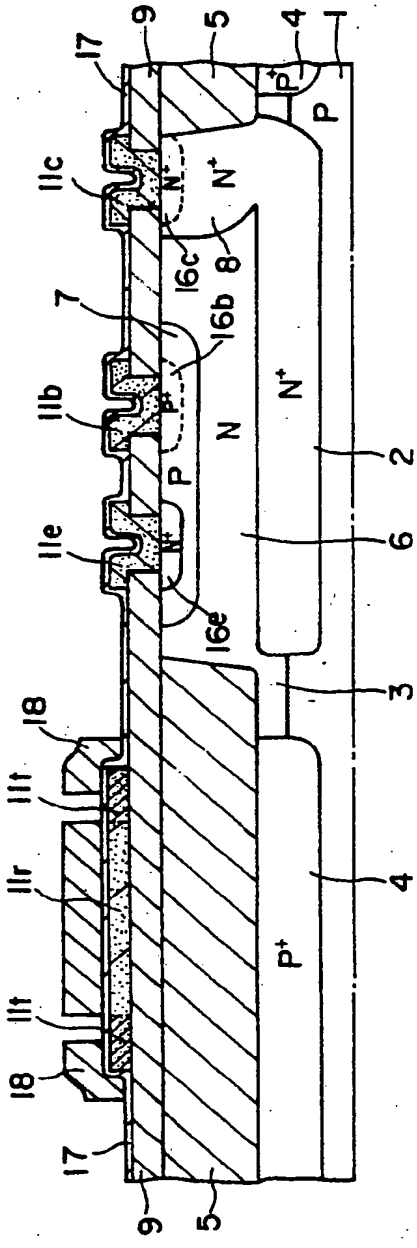
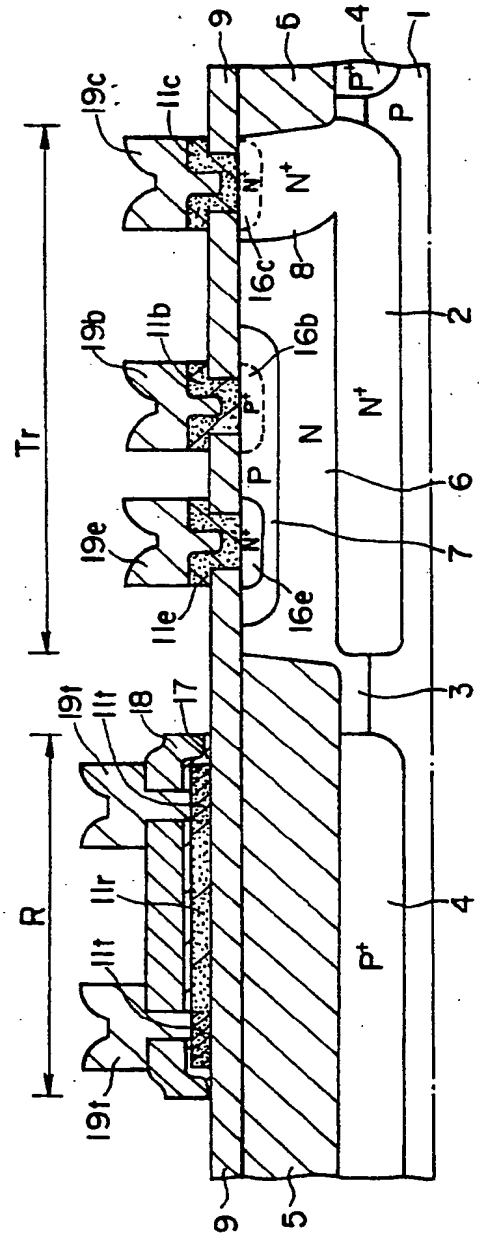


FIG. 1I

FIG. IJ



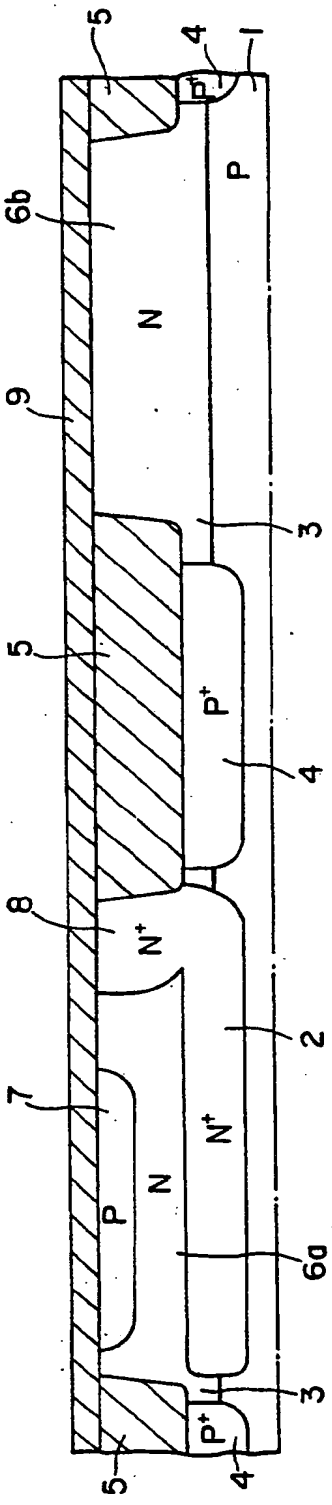


FIG.2A

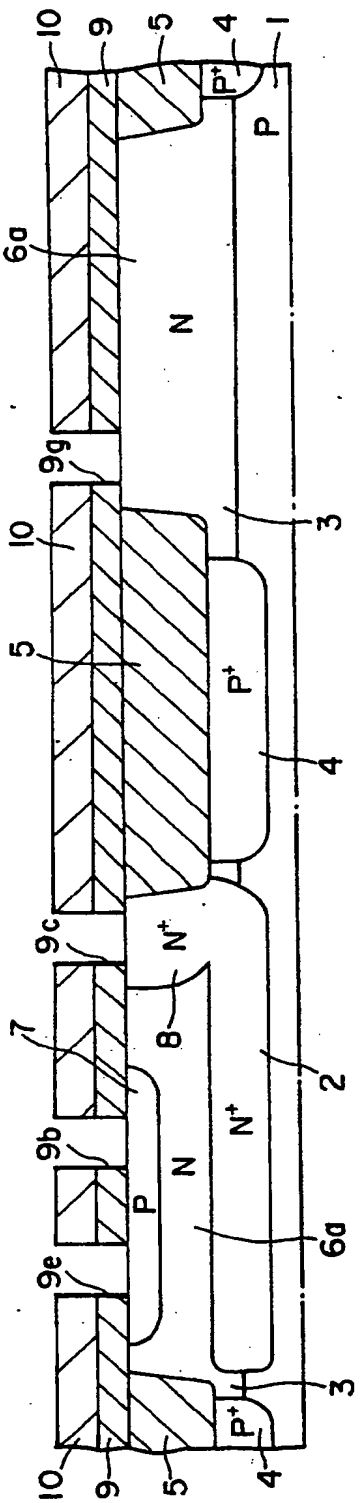


FIG.2B

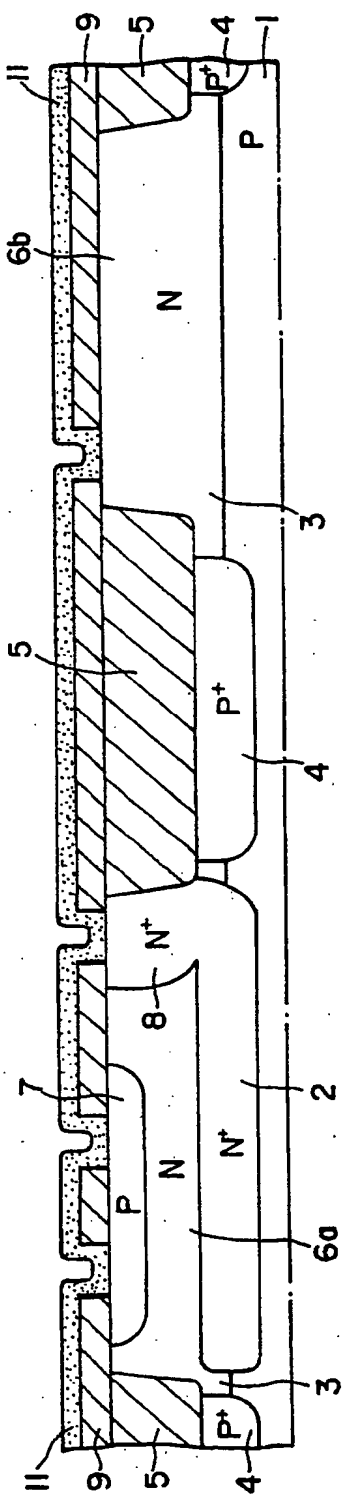


FIG.2C

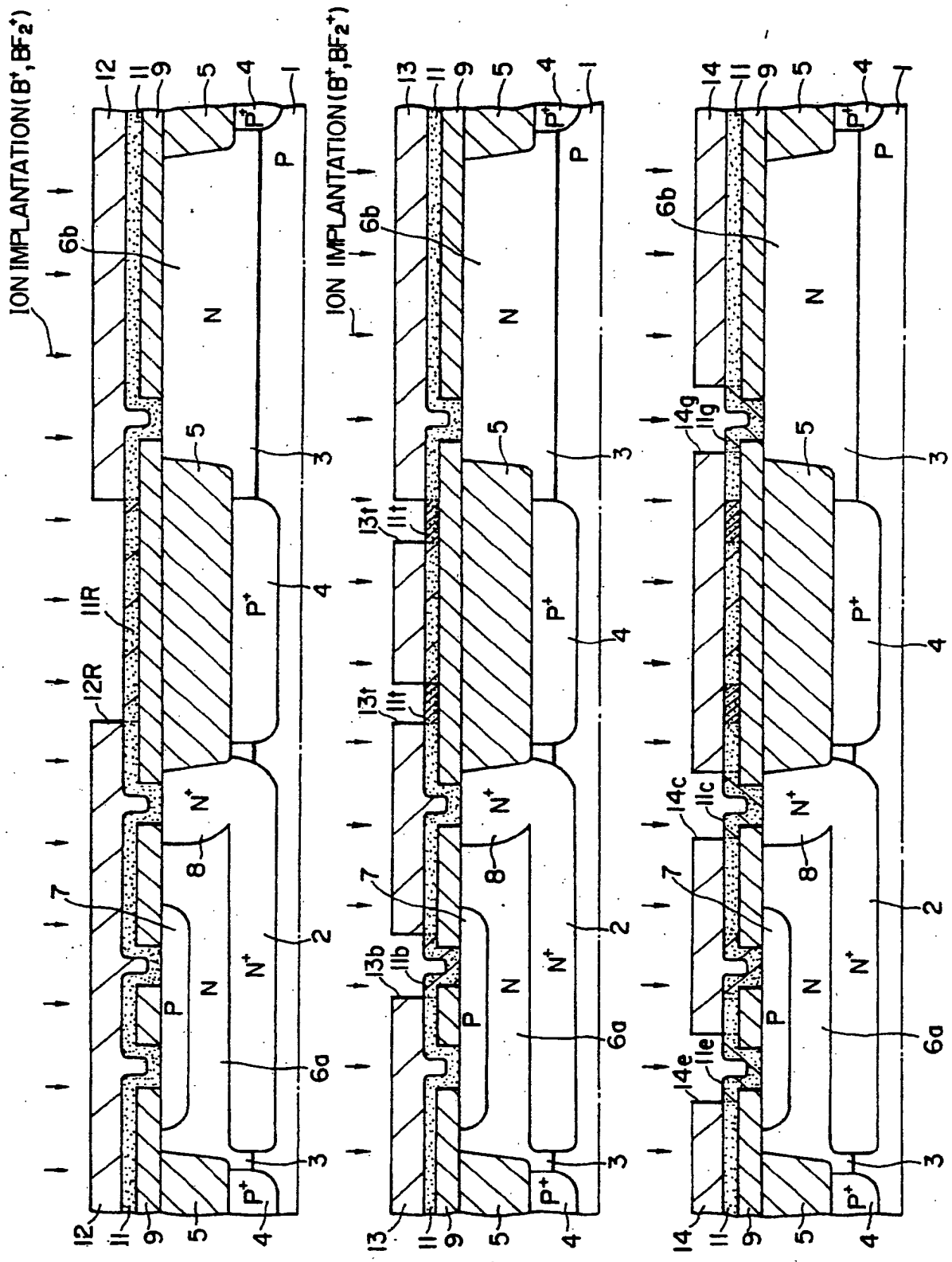


FIG.2D

FIG.2E

FIG.2F

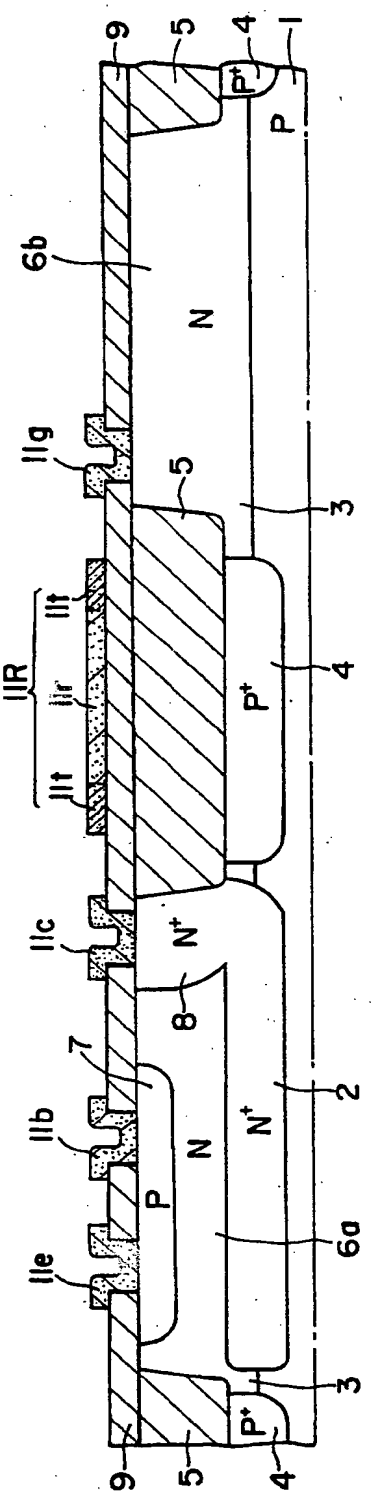


FIG.2G

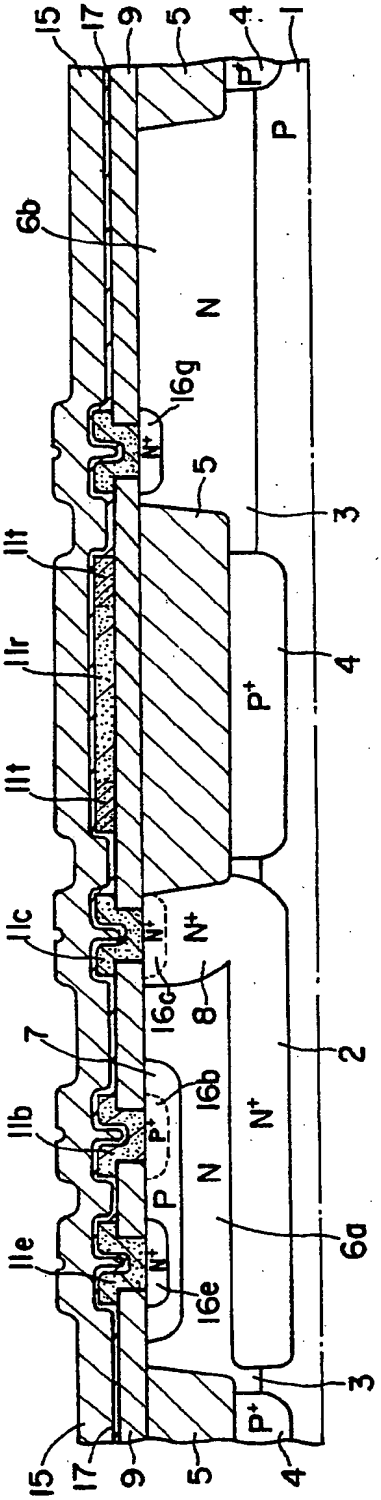


FIG.2H

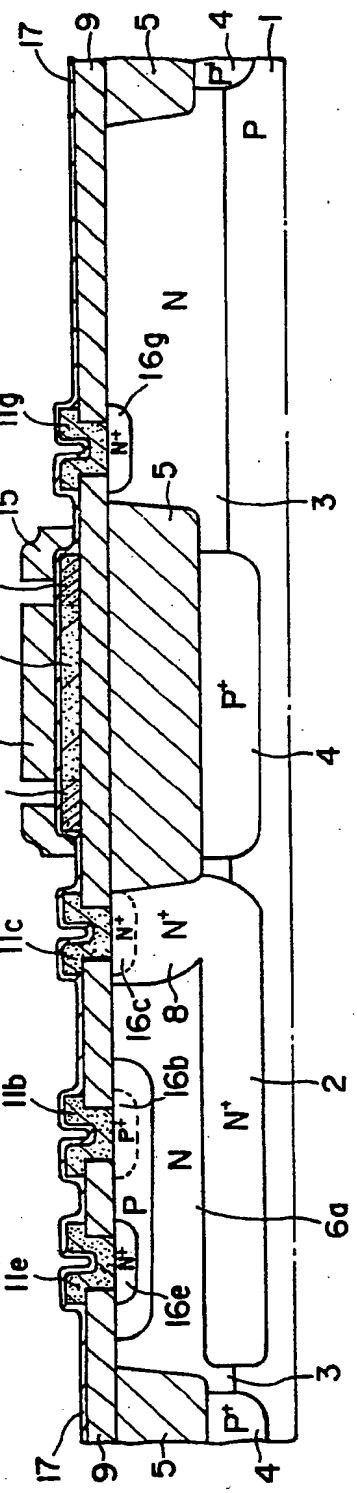


FIG.2I

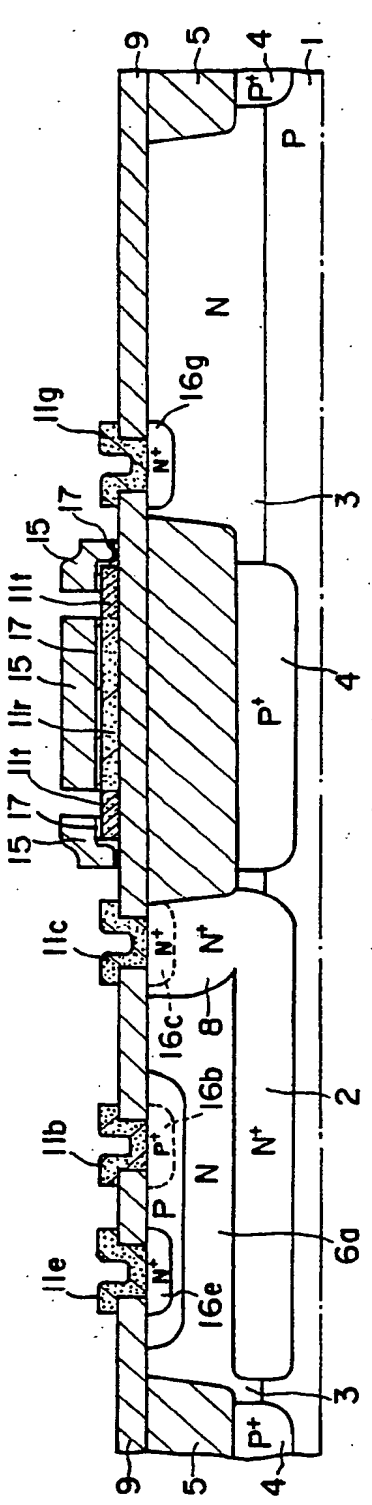


FIG.2J

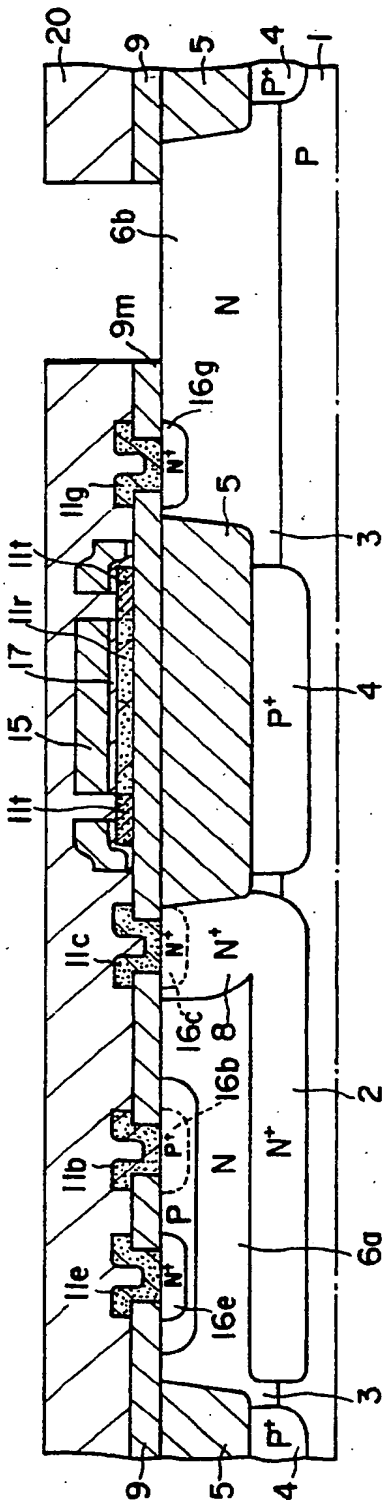


FIG.2K

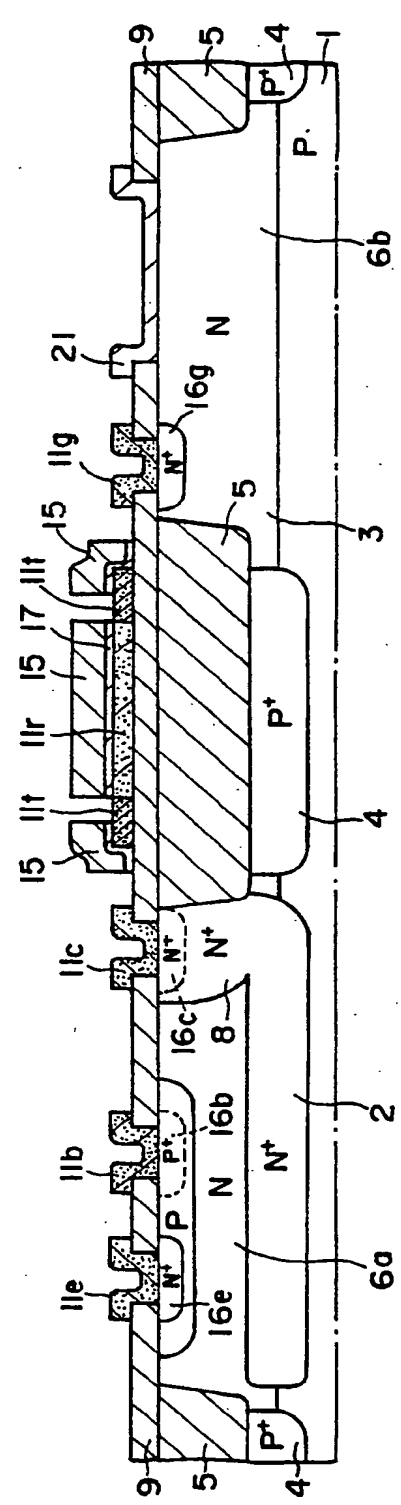


FIG.2L

FIG. 2M

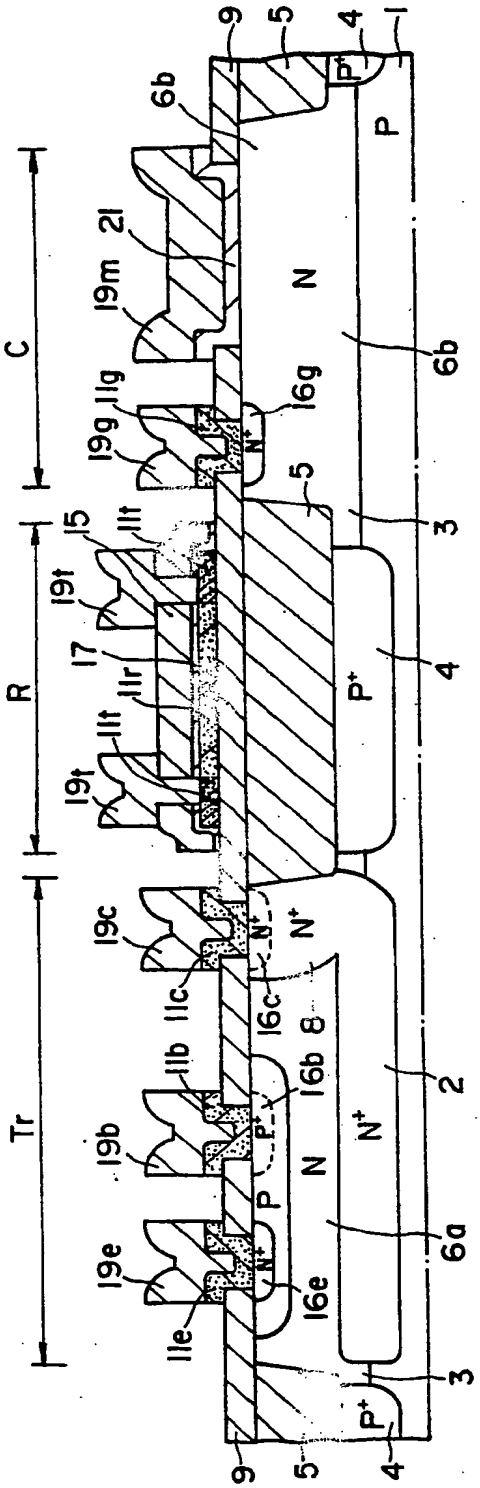


FIG.3A

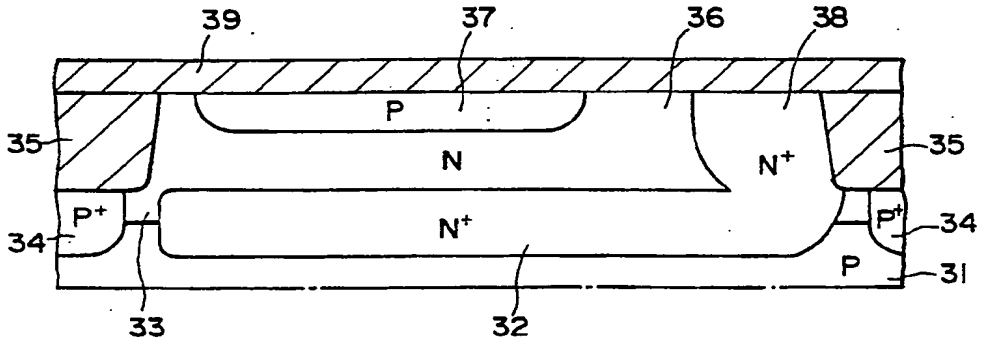


FIG.3B

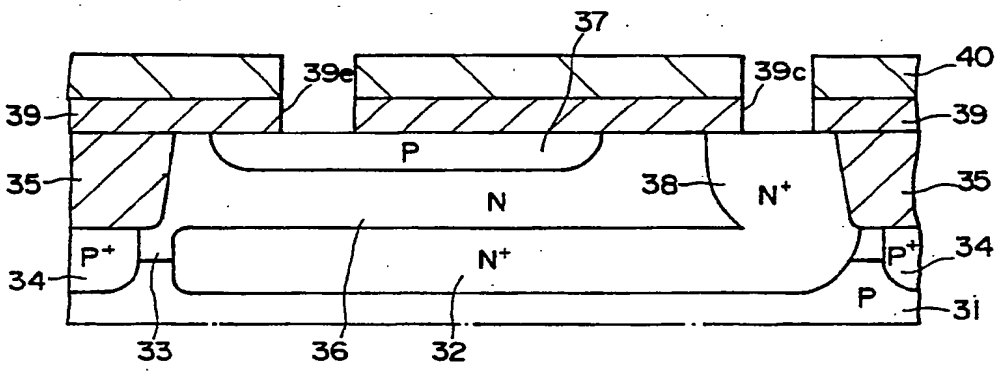


FIG.3C

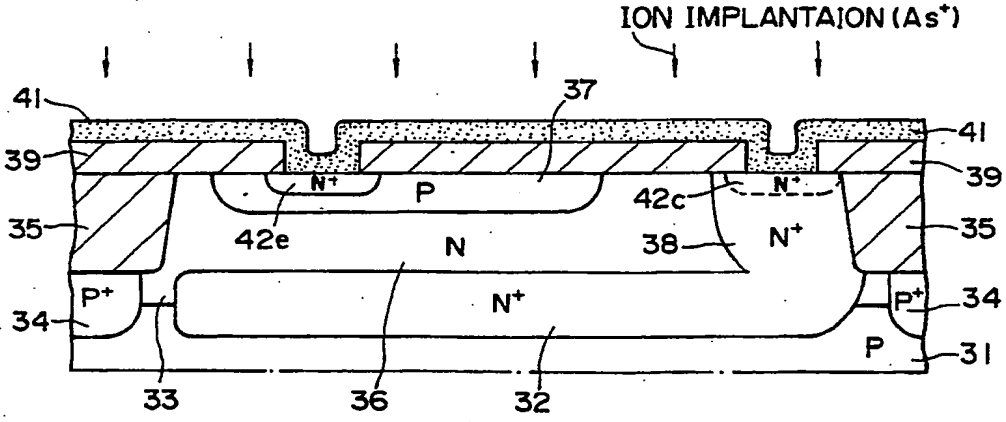


FIG.3D

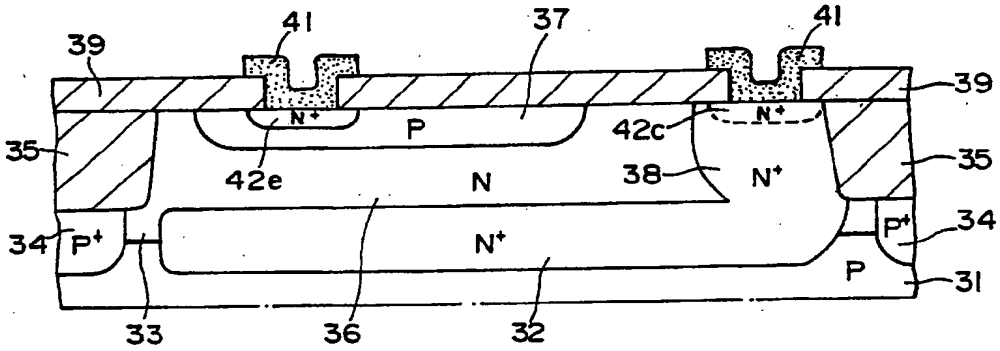


FIG.3E

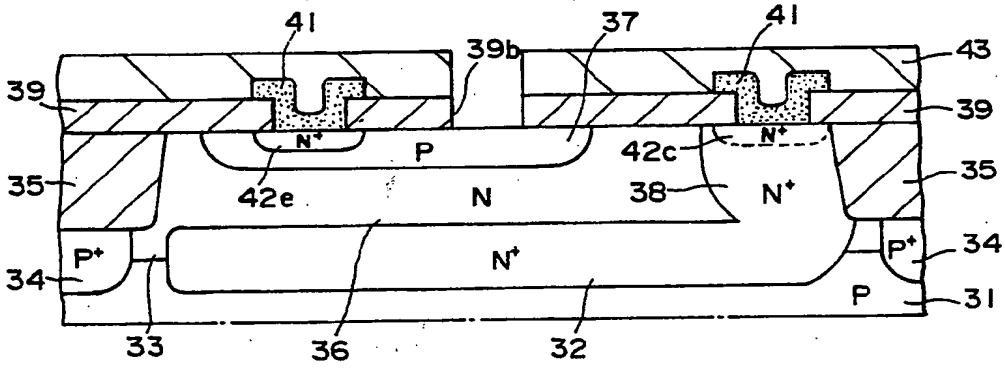
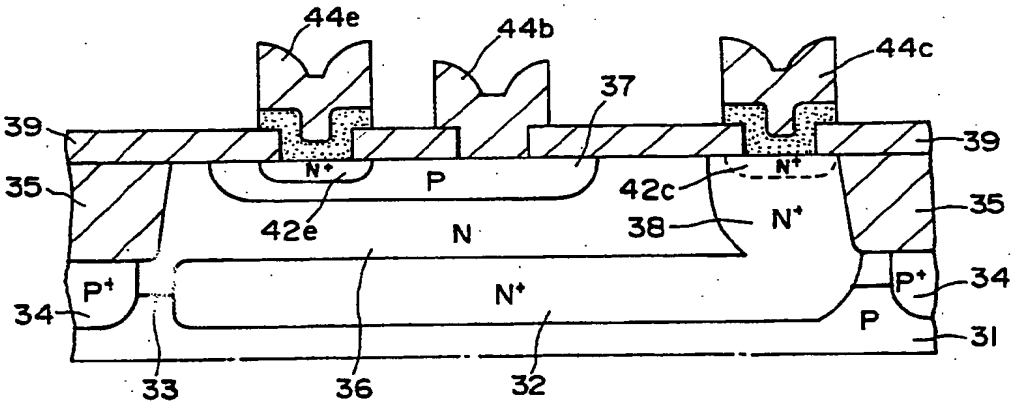


FIG.3F



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(54) **Manufacture of semiconductor devices.**

(57) A method of manufacturing a semiconductor device comprises forming a plurality of openings (9e, 9b, 9c) for ohmic contact portions at the same time, then forming a semiconductor layer (11) on an entire surface including the openings, and selectively introducing impurities by ion implantation into the contact portions and isolated other element regions (11e, 11b, 11c, 11t, 11R) of the semiconductor layer (11), thereby producing a transistor (Tr) and at least one other element (R; R, C).

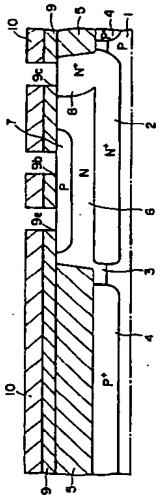
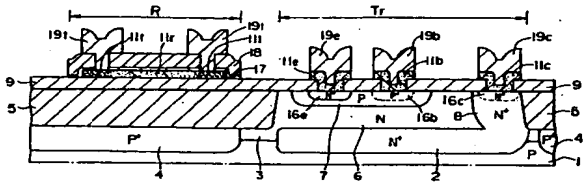


FIG. IB

FIG. IJ



EP 0 404 464 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

DOCUMENTS CONSIDERED TO BE RELEVANT

EP 90306591.0

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP - A - 0 007 923 (IBM) * Claims; fig. *	1-3	H 01 L 21/331 H 01 L 21/82
A	EP - A - 0 183 204 (HITACHI) * Claims; fig. *	1-3	
A	US - A - 4 471 525 (Y. SASAKI) * Claims; abstract *	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 01 L 21/00

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	13-05-1992	HOFBAUER

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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